

Faculty of Engineering & Technology Electrical & Computer

Engineering Department

ENCS3390 Operating Systems

Project: Virtual Memory Management Simulation

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Abstract:

In this project, we implemented a virtual memory management simulator with page replacement algorithms, which were, FIFO and LRU, the odd ones in the algorithms list in project description (1,3) based on the max value of the least significant digit of the team ID numbers.

Theory:

The First In First Out (FIFO) page replacement algorithm operates by replacing the frame which was loaded to memory at the earliest time. Thus, when the allocated pages for a process are full, the algorithm replaces the earliest loaded frame with the frame requested from the hard disk. The second page replacement algorithm, Least Recently Used (LRU) operates by replacing the frame which was least recently accessed with the one requested from the hard disk.

The programmed simulation is multithreaded, where each process is simulated on a separate thread.

How to run this code:

First, you can generate a new file and enter the number of processes, the size of physical memory in frames, and the minimum number of frames per process as in figure 1, or you can browse and specify an existing file.



Figure 1



Second, choose the page replacement algorithm you need as in Figure 2, and start the simulator.

Figure 2

Virtual Memory Simulation	_	
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Browse File Generate File First In First Out	•	
Input File Path: C:\Users\islam\eclipse-workspace\test\Input.txt	Process Name	PID
Number of Processes = 7 Memory Size = 50	▶ process0	0
Max Frames per Process = 5 Run Test	process1	1
	process2	2
Running First In First Out Algorithm:	▶ process3	3
New thread: Thread[process0,5,main]	▼ process4	4
process0 : [W0, R4, W5, W2, R0, W8, R8, R2, R5, W7, W5, W6]	W3	569
Current Allocated Frames = [*, *, *, *, *]	W1	569
	W0	569
process1 ; [W2, W2, R1, R2, R1, W1, R1, W2, R0, R2, R3]	W0	569
New thread: Thread[process2,5,main]	W1	569
Number of Pager = 4	W3	569
Current Allocated Frames = [*, *, *, *, *] Restart	R6	569
process2 : [R2, R3, W2, R5, R3, R4, W2, W4, W3, W3, R0]	RO	569
Number of Pages = 6 Current Allocated Frames = 1* * * * *1	W1	569
	W4	569
Total Nite 45 Total Disk Accesses (Total faults) 77	W3	569
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Show Memory Show Process Details		

Figure 3 : creation of a new thread.

Virtual Memory Simulation	_		×
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Browse File Generate File First In First Out	•		
New thread: Thread[process5,5,main] process5 : [R3, W2, R3, R2, W1, W2, W0, R2, W1, R2, W4, R3, R2, R4] Number of Pages = 5 Current Allocated Frames = [*,*,*,*] New thread: Thread[process6,5,main] process6 : [R1, R4, R2, W1, W4, R1, R3, R2, R4, R1, W1, W0, W3] Number of Pages = 5 Current Allocated Frames = [*,*,*,*] [process3:W6] : Miss Dirty = false Current Allocated Frames = [R2, *, *,*,*] [process5:W6] : Miss Dirty = true Current Allocated Frames = [W0, *,*,*,*] [process5:W3] : Miss Dirty = false Current Allocated Frames = [W0, *,*,*,*] [process5:W3] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process5:R3] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process5:R3] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process5:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W3, *,*,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W0, R4, *,*,*] [process6:R4] : Miss Dirty = false Current Allocated Frames = [W2, *,*,*,*]	 Process Name process0 process1 process2 process3 process4 process5 process6 	PID 0 1 2 3 4 5 6	
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Show Memory Show Process Details			

Figure 4: how the simulation goes.

mory Allocation					-
Process Name	Process ID	Frame Number	Valid	Dirty	_
process0	628	4	false	false	_
process0	628	3	false	true	
process0	628	2	false	false	
process0	628	1	false	true	
process0	628	7	false	false	
process0	628	0	false	true	
process0	628	6	false	true	
process1	495	2	false	false	
process1	495	0	false	true	
process1	495	4	false	false	
process1	495	5	false	true	
process1	495	3	false	false	
process1	495	1	false	true	
NULL	-1	-1	false	false	
process2	893	4	false	false	
process2	893	3	false	true	~
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Figure 5: memory table.

Virtual Memory Simulation		-	
			х
Browse File Generate File	First In First Out	•	
Running on [process2]:	Start	Process Name	PID
Running FIFO Algorithm:		process0	o ^
[process2:R2] Miss Dirty = true Current Allocated Frames = [R2, *, *, *, *]	Run Test	process1	1
[process2:R3] Miss Dirty = true Current Allocated Frames = [R2, R3, *, *, *] [process2:W2] Hit Dirty = true Current Allocated Frames = [W2, R3, *, *, *]	V FIFO	▼ process2	2
[process2:R5] Miss Dirty = true Current Allocated Frames = [W2, R3, R5, *, *]		R2	181
[process2:R3] Hit Dirty = true Current Allocated Frames = [W2, R3, R5, *, *] [process2:R4] Miss Dirty = true Current Allocated Frames = [W2, R3, R5, R4, *]		R3	181
[process2:W2] Hit Dirty = true Current Allocated Frames = [W2, R3, R5, R4, *]		W2	181
[process2:W4] Hit Dirty = true Current Allocated Frames = [W2, R3, R5, W4, *]		R5	181
[process2:W3] Hit Dirty = true Current Allocated Frames = [W2, W3, K5, W4, ^] [process2:W3] Hit Dirty = true Current Allocated Frames = [W2, W3, R5, W4, *]		R3	181
[process2:R0] Miss Dirty = true Current Allocated Frames = [W2, W3, R5, W4,		R4	181
R0]	Clear	W2	181
Running LRU Algorithm:		W4	181
[process2:R2] Miss Dirty = false Current Allocated Frames = [R2, *, *, *, *]	Restart	W3	181
[process2:R3] Miss Dirty = false Current Allocated Frames = [R2, R3, *, *, *] [process2:W2] Hit Dirty = true Current Allocated Frames = [W2, R3, *, *, *]		W3	181
[process2:R5] Miss Dirty = false Current Allocated Frames = [W2, R3, R5, *, *]		RO	181 🛛
[process2:R3] Hit Dirty = false Current Allocated Frames = [W2, R3, R5, *, *]	~	process3	3
Total Hits 45 Total Disk Accesses (Total faults) 77		process4	4 🗸
Show Memory Show Process Details		<[$ \rightarrow $

Figure 6: shows run test for process 2 using FIFO algorithm.

Virtual Memory Simulation			-		×
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Browse File Generate File	First In	First Out	•		
[process2:R0] Miss Dirty = true Current Allocated Frames = [W2, W3, R5, W4,	^		Process Name	PI	D
R0]			 process0 	0	Â.
Running LRU Algorithm:		Run Test	process1	1	
[process2:R2] Miss Dirty = false Current Allocated Frames = [R2, *, *, *, *] [process2:R3] Miss Dirty = false Current Allocated Frames = [R2, R3, *, *, *]			▼ process2	2	
[process2:K3] Miss [Dirty = Table Current Allocated Frames = [K2, K3, *, *, *]			R2	181	
[process2:R5] Miss Dirty = false Current Allocated Frames = [W2, R3, R5, *, *]			R3	181	
[process2:R3] Hit Dirty = false Current Allocated Frames = [W2, K3, K5, ^, ^] [process2:R4] Miss Dirty = false Current Allocated Frames = [W2, R3, R5, R4, *]			W2	181	
[process2:W2] Hit Dirty = false Current Allocated Frames = [W2, R3, R5, R4, *]			R5	181	
[process2:W4] Hit Dirty = true Current Allocated Frames = [W2, R3, R5, W4, *] [process2:W2] Hit Dirty = true Current Allocated Frames = [W2, W2, R5, W4, *]			R3	181	
[process2:W3] Hit Dirty = true Current Allocated Frames = [W2, W3, R5, W4,] [process2:W3] Hit Dirty = true Current Allocated Frames = [W2, W3, R5, W4, *]			R4	181	
[process2:R0] Miss Dirty = false Current Allocated Frames = [W2, W3, R5, W4,		Clear	W2	181	
R0]			W4	181	
FIFO Disk Acesses: 8		Restart	W3	181	
FIFO Hits: 6			W3	181	
LRU Hits: 6			RO	181	
	U V		process3	3	
Total Hits 45 Total Disk Accesses (Total faults) 77			process4	4	~
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Show Memory Show Process Details					

W3] Hit | Number of faults = 7 | Current Allocated Frames = [W2, W3, R5, W4, *]

Figure 7: shows run test for process 2 using LRU algorithm.

Conclusion:

This project simulated some of the most important parts of an operating system and its key concepts. It demonstrated multithreading, CPU scheduling, memory page replacement algorithms, and hard disk access. In addition to the simulation, the project included the programming and design of a graphical user interface. Thus this project demonstrated the development of a useful, complex, application, from the theoretical phase, to the implementation, to the final stages of development.